Copper (Cu) is becoming the interconnect metal of choice and is rapidly replacing Aluminium alloys (Al/Cu) in the Integrated Circuit (IC) industry. However, mechanical reliability issues, such as those related to thermal strain are a major concern. This study aims to evaluate and compare stress distributions in Si wafers due to the electroless Cu interconnect process with varying geometrical line widths in IC processing using White Beam Synchrotron X-Ray Topography (WBSXRT), Micro-Raman Spectroscopy (MRS) and Finite Element Modelling (FEM). 100 nm of Ti is used as a barrier layer and 20 nm of sputtered Cu is used as a seed layer. A 500 nm layer of electroless Cu was subsequently deposited on patterned Si wafers with 4, 6, 8, 10, 20, 40, 60 and 100 µm line widths using a lift-off patterning technique.

The presence of distinct orientational contrast observed in section topographs suggests that the strain fields in the Si substrate reach values as high as ca. 100 MPa near the metal edge. The stress magnitudes in the underlying Si as a function of individual line widths were measured using MRS. Compressive stresses of ~100 MPa were found in the Si wafer near the line edges when the width is less than 10 µm. The stresses changed to tensile with a magnitude of the order of 100 MPa at metal widths of 10-60 µm and decreased to ~50 MPa for 100 µm widths. The FEM analysis confirmed this tendency.

Large area back-reflection WBSXRT (LA-BRT) revealed that strain fields in the Si due to the Cu metallisation were relieved when the sample was heated to 400°C. Nevertheless, the strain relief was not complete at this temperature.

![Fig. 2](image)

**Fig. 2:** LA-BRTs of strain relief due to annealing at (a) 100, (b) 200, (c) 300 and (d) 400 °C.

When the samples are returned to room temperature, the MRS data confirms that the strain in the Si near the metal edges become more compressive than in the unannealed case. The stress frozen in the Si during processing is now being partially relieved after increasing the temperature. However, the strain fields along the edge of copper lines still can be observed in this image. The stress distributions in Si wafers due to the Cu metallisation for both unannealed and annealed cases were evaluated using micro-Raman spectroscopy. For example, a comparison of the normal stress ($\sigma_{xx}$) in
the Si adjacent to the metal edge from the experimental MRS data, the calculated FEM distribution and empirical estimates of

\[ \sigma_{xx} = 139.5 - 195.5 \exp\left(-\frac{\text{Cu line width}}{2.3}\right) \]  
(Eq. 6-32: based on the FEM data)

\[ \sigma_{xx} = 115.6 - 281.4 \exp\left(-\frac{\text{Cu line width}}{5.5}\right) \]  
(Eq. 6-33: based on the MRS data)

is shown in Figure 3.

Graham et al. [1] found that copper self-annealing is a function of the copper line widths and that the smaller Cu line width requires a higher activation energy to achieve full recrystallisation. The physical limitation of the Cu lines together with the self-annealing phenomenon, could explain the line width vs. stress dependency of Figure 3, since the recrystallisation process could not occur when the Cu line width becomes very small as the density of grains per volume is not large enough for the recrystallisation process [1-3]. Therefore, the stress in the Si due to small Cu line widths is high, whereas the self-annealing process relieves the stress in the Si due to wider Cu lines.

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